Harmonic Load/Source Pull Strategies For High Efficiency PAs Design

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***Abstract* – An advanced load/source pull bench has been used in conjunction with harmonic tuning techniques for accurate and effective power amplifier design. The optimization strategy is presented together with the measured results obtained with a medium power 1-mm MESFET.**

I INTRODUCTION

The design of power amplifier (PA) requires non linear techniques to account for phenomena due to the hard limits of the active device. Pushed by the high level performances required by modern applications, different design strategies have been proposed. In particular, to improve both output power and conversion efficiency, harmonic tuning strategies have been addressed and successfully applied at microwave frequencies [1]. From a practical point of view, two different approaches are available based on simulation or experimental results. In the former case a full non linear model for the active device is required, joined with nonlinear analysis algorithms. The main difficulty of this approach is related to the use of appropriate non linear model, to predict results with a good accuracy. The latter approach is based on experimental measurements, namely load/source pull techniques, in which the actual active device is fully characterized in terms of output power, matching impedances, efficiency and any other required performance, by means of an exhaustive and intensive measurement activity [2]. It is clear that the experimental approach represents a direct solution, since the actual device is characterized in real time (no models are required) and design quantities are readily available.

Nevertheless, in both cases (i.e. simulations or experiments) if harmonic tuning approaches needs to be investigated, some consideration must be applied, exploiting the theoretical results proposed in the past by means of simplified analysis [3].

The aim of this contribution is to present the combination of an advanced harmonic load pull test bench with harmonic tuning guidelines, thus forming an accurate and effective tool for power amplifier design.

II NON LINEAR TEST BENCH

The measurement set-up, already proposed in [2], that combines S-parameter capability, real-time load- and source-pull (single tone or harmonic) with time domain waveform measurements has been extended to intermodulation measurements. Any linear Vector Network Analyzer (VNA) with at least two samplers can be used as linear receiver, while a Microwave Transition Analyzer (MTA) is used as a non-linear receiver, measuring the phase relationships between harmonics of the signals at the Device Under Test (DUT) ports. The set-up is completed with two independently controlled active loops (more loops could be added). The loops can be set at the input or output of the device, and tuned both for single tone and harmonic measurements. A simplified scheme of the test bench is shown in Fig. 1.

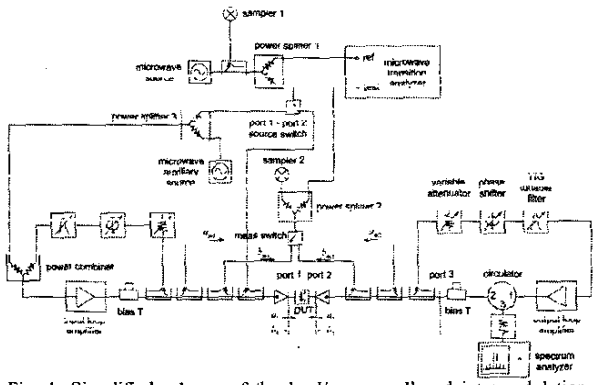

Fig. 1: Simplified scheme of the load/source-pull and intermodulation set-up, with waveform measurement capabilities.

The linear and non-linear receivers are simply combined by means of two power splitters. In other words, the two receivers work in parallel on the same DUT. The information achievable with this system are therefore:

- input and output reflection coefficients, at fundamental and harmonics
- source reflection coefficients ("port 1-port 2 source switch" allows RF switching technique [4]), at fundamental and harmonics
- input and output power, at fundamental and harmonics
- power added efficiency
- intermodulation products

This is a more effective (but also more expensive) technique if compared to other similar systems [5], where only an MTA is used as a receiver: the flexibility, accuracy and speed of a real-time load-pull and S-parameter test-set is combined with the additional waveform information provided by the MTA. Indeed, after the calibration phase, the slower MTA measurements are performed only if and when needed. The quantities of interest and performances are measured with higher speed and accuracy with the VNA. Moreover, the simultaneous presence of the two receivers allows simple verification capabilities of both time/frequency domain measurements.

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The general calibration procedure [2] is an extension of the on-wafer techniques described in [6,7] and improved for coaxial MTA based system in [5]. During calibration, "port1-port2 source switch" is connected, as in figure, in cascade to "power splitter 1", but its ways are connected at the input and output of the DUT, excluding the two bias T. Thus, S-parameter calibration of the system is performed (with any two-port technique, e.g. TRL), and the linear relations (or error boxes) between a_1, b_1, a_2, b_2 (waves at the DUT ports) and the measured waves a_{m1}, b_{m1}, a_{m2}, b_{m2} are found. Then, coaxial "port 3" is used [6] for absolute power calibration, connecting three known coaxial standards and a Power Meter.

Finally, in a similar way, absolute phase calibration at the DUT ports is performed by connecting "port 3" to MTA "test" port. During calibration and measurements, the MTA reference channel is connected to the source signal.

III Experimental Description

The test device is a medium power MESFET (10x100μm) by AMS, which has been also modeled by a full non linear model, employing neural network concepts [8]. The device knee voltage is V_k=0.9V, the dynamic drain-source resistance is r_{ds}≈150Ω and its maximum intrinsic drain current is I_{max}=220mA. A drain bias voltage of 5V has been selected, while the gate bias voltage has been chosen at –2V, corresponding to an intrinsic drain dc current I_{DC}≈40mA. An operating frequency f_o @1GHz has been chosen while, for the intermodulation measurements, the second source has been selected 100kHz higher than f_o.

To perform a multi-harmonic load pull, the test bench depicted in Fig. 1 has been adopted, in which one active loop should be added to control each harmonic termination. Consequently, to avoid test bench cost and complexity increase, the number of active loops has been minimized. Moreover, a measurement procedure is required, as contrasted to a blind optimization, to reduce time consumption and to bounce sub-optimum results.

In this paper, combining the theory proposed in the past [1,3] by means of simplified device model, with the experimental results available with the test bench shown in Fig. 1 on an actual device, a suitable measurement procedure is presented. Moreover, to reduce complexity and cost, only one active loop has been adopted. In this way only a single termination, either at the input or at the output port, at fundamental or harmonic frequencies, has been controlled each time.

The proposed measurement procedure can be summarized in the following steps:

A. load pull *@fo* to find the optimum load $Z_{L@fo}$ at the output port (matching the input @fo);
B. source pull *@2fo* to analyze the effects of the load at the input port at the second harmonic $Z_{S@2fo}$;
C. load pull *@fo to correct the output load* ($Z_{L@fo}^*$) *and to* further increase device performances.

Usually, if the load pull test bench has harmonic tuning capabilities, the first 2 steps only are performed, neglecting the benefits related to the third one, as shown in the following.

A. Step 1: Load Pull on $Z_{L@fo}$

The first step is a traditional load pull on output termination *@fo*, to obtain the optimum load $Z_{L@fo}$ and the input matching impedance $Z_{S@fo}$ at fundamental frequency. In this step the harmonic termination effects are not explored, i.e. the harmonic terminations can be fixed at a given value (short circuit if possible or 50Ω) without tuning. In this experiment for simplicity, standard 50Ω loads have been presented to the active device at all harmonic terminations. To further reduce time effort, a $Z_{L@fo}$ starting point can be estimated by means of simplified considerations inferred with a linearized active device model [9]. After that, on the test bench the $Z_{L@fo}$ values can be tuned changing the parameters of the fundamental output active loop, thus mapping the Smith chart around the starting point, until an optimum is reached In this experiment the optimum output load value $\Gamma_{L@fo}$≈0.131$e^{j\cdot 143.45°}$ has been determined.

Output power (P_{out}) and drain efficiency (η) are shown in Fig. 2 *vs.* available input power (P_{av}), compared with the simulated results obtained through a full non linear analysis. Drain current and voltage waveforms @-1dB compression, measured with the proposed test bench are plotted in Fig. 3, together with the results of a full nonlinear simulation.

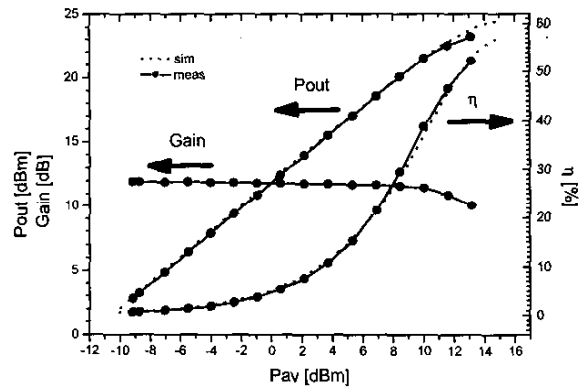

Fig. 2: Single-tone measured performances (dotted lines) compared with simulation results (solid lines) @1GHz

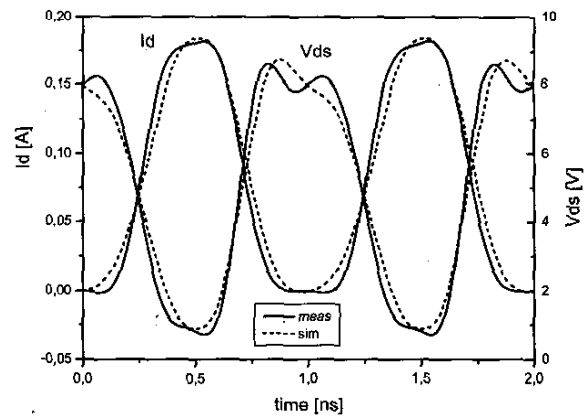

Fig. 3: Measured (solid lines) *vs.* simulated (dot lines) time domain waveforms for voltage and current @ -1dB compression.

B. Source Pull on $Z_{S@fo}$

The second step is a source pull in order to investigate the effects of the input second harmonic termination $Z_{S@2fo}$ [3]. In particular, exploiting the input non linear effects by a proper choice of $Z_{S@2fo}$ it is possible to modify the phase relationships

between the drain current harmonic components generated at the output (i.e. 1st vs 2nd) [1]. In this way output harmonic tuning strategies can be applied to properly shape the output drain voltage waveforms, both reducing the dissipated power on the device and increasing the power delivered from the device, thus increasing efficiency.

For this purpose, a fixed input drive level has been assumed, corresponding to -1dB compression (P_{av}≈11.5dBm in the experiment), and all the possible (passive) values for $Z_{S@2f_0}$ have been investigated, leaving all the other terminations at the values of prior step.

The measured contour plot of drain efficiency (η) as a function of the $Z_{S@2f_0}$ is shown in Fig. 4. From this picture it is possible to note that efficiency reaches the maximum value of η=49% (in the following referred to as *case 1*) corresponding to an improvement of 6.5% with respect to the starting value; moreover, a minimum point can also be observed (*case 2*), which corresponds to η=36% (i.e. a 22% of decrease).

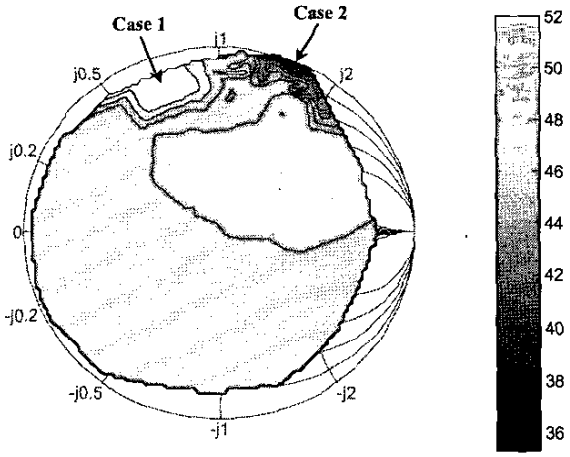

Fig. 4: Measured contour plot of drain efficiency *vs.* $Z_{S@2f_0}$.

Output power and efficiency measurements obtained in case 1 (maximum η) and 2 (minimum η) are shown in Fig. 5, while the corresponding output voltage and current waveforms are reported in Fig. 6. From this figure it is possible to note that drain voltage harmonic components, and in particular fundamental and 2nd harmonic ones, have different phase relationships in the two cases: they are wrong in phase in *case 2*, thus implying an improper v_{ds} wave shaping, decreasing the device performances; otherwise, in *case 1*, the drain voltage harmonic components are properly combined, resulting in improved device performances.

To completely clarify the effects of the input second harmonic terminations, also intermodulation measurements have been performed, utilizing two sources at f_1=1GHz and f_2=f_1+Δf with Δf=100kHz, obtaining the results shown in Fig. 7, where

$$IM3 = \frac{Pout(2f_2 - f_1)}{Pout(f_1)} \quad (1)$$

The *IM3* results show that $Z_{S@2f_0}$ affects also the device IMD distortion, as already stressed in [10].

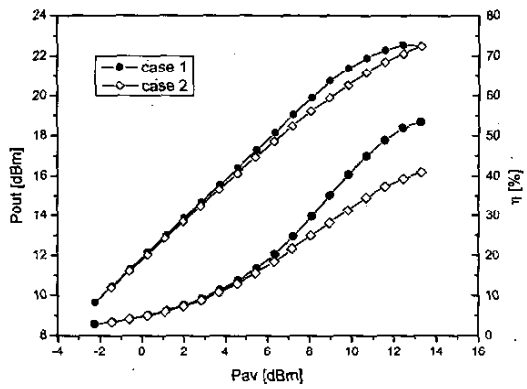

Fig. 5: Output power and efficiency measured for case 1 and 2.

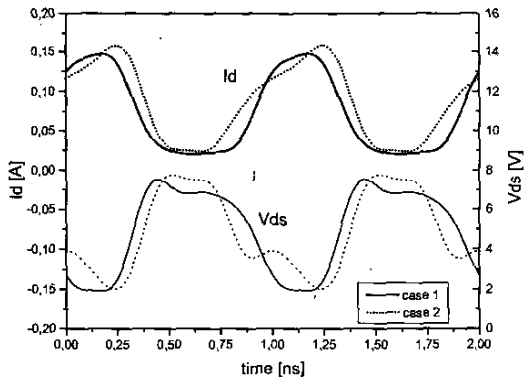

Fig. 6: Output voltage and current waveforms corresponding to case 1 and case 2.

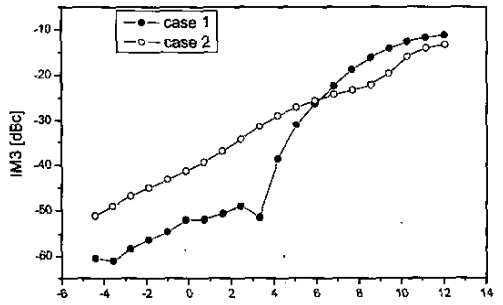

Fig. 7: Two-tone performances measured for case 1 and 2, corresponding to maximum and minimum values for drain efficiency.

C. *Load Pull on $Z_{L@f_0}$ again*

Finally, to show that further improvements can be obtained increasing the fundamental output load (i.e. its resistive part) [1], a load pull has been again performed on $Z_{L@f_0}$ leaving all the other terminations unchanged from the previous case.

The final optimum load $Z_{L@f_0}^*$ is shown in Fig. 8 while the drain efficiency is shown in Fig. 9.

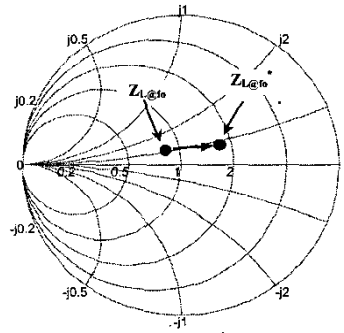

Fig. 8:Initial ($Z_{L@fo}$) and final ($Z_{L@fo}^{*}$) optimum output load at fundamental

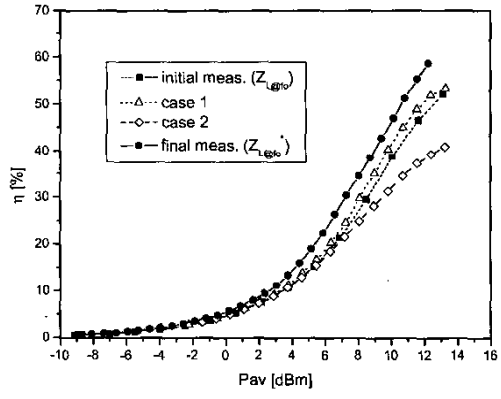

Fig. 9: Efficiency performances measured during the three step of the experiment.

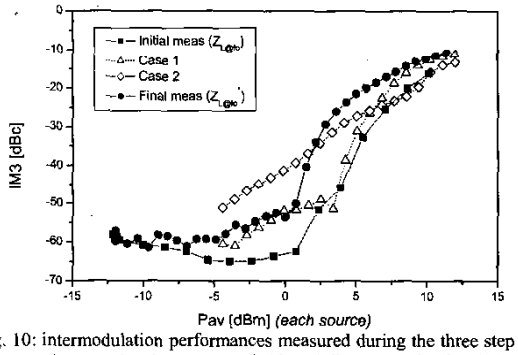

Fig. 10: intermodulation performances measured during the three step of the experiment. Fig. 11: measured (dotted lines) vs simulated (solid lines) intermodulation measurements for 2 tones @1GHz and @1.0001GHz.

The final results exhibit an increase in maximum efficiency from 53.4% (maximum obtained at step 2) to 66.4%, i.e. a further increase of about 24%.

The impedance value resulting from the preliminary procedure ($Z_{L@fo}$) is close to the ideal tuned load value computed from [9]. Moreover, the final value ($Z_{L@fo}^{*}$) is in the proper ratio to $Z_{L@fo}$ as forecasted in [1].

IV Conclusions

The combination of an advanced harmonic load/source pull test bench with harmonic tuning guidelines has been presented. The proposed three-step strategy has demonstrated major benefits with respect to a blind load pull optimization scheme, resulting in increasing performances both in terms of output power and efficiency for a sample medium power MESFET.

References

[1] P.Colantonio, F.Giannini, G.Leuzzi, E.Limiti, "Multi Harmonic Manipulation for Highly Efficient Microwave Power Amplifiers," *International Journal of RF and Microwave Computer-Aided Engineering*, Vol.11, N°6, Nov. 2001, pp. 366-384.

[2] A.Ferrero, V.Teppati, "A complete measurement test-set for non-linear device characterization," *58th ARFTG Conference Digest*, San Diego, USA, November 2001.

[3] P.Colantonio, F.Giannini, G.Leuzzi, E.Limiti, "Harmonic Tuned PAs Design Criteria," *2002 IEEE MTT-S Symposium Digest*, Seattle, WA, June 2002, vol.3, pp.1639-1642.

[4] G.Berghoff, E.Bergeault, B.Huyart, L.Jallet, "Automated characterization of HF power transistor by source-pull and multiharmonic load-pull measurements based on six-port techniques," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-46, pp. 2068-2073, December 1998.

[5] J.Benedikt, R.Gaddi, P.J.Tasker, M.Goss, "High-power time-domain measurement system with active harmonic load-pull for high-efficiency base-station amplifier design," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-48, Issue 12, pp. 2617-2624, December 2000.

[6] A.Ferrero, U.Pisani, "An improved calibration technique for on-wafer large-signal transistor characterization," *IEEE Trans. Instrum. Meas.*, vol. IM-47, pp. 360-364, April 1993.

[7] G.Kompa, F.van Raay, "Error-corrected large-signal waveform measurement system combining network analyzer and sampling oscilloscope capabilities," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-38, Issue 4, pp. 358-365, April 1990.

[8] F.Giannini, G.Leuzzi, G.Orengo, P.Colantonio, "Neural-Based Large-Signal Device Models Learning First-Order Derivative Parameters for Intermodulation Distortion Prediction," *Proc. of the European Gallium Arsenide Applications Symposium*, Milano, Italy, September 2002, pp.197-200.

[9] H. Kondoh, "FET power performance prediction using a linearised device model," *1989 IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 569-572.

[10] M.R.Moazzam, C.S.Aitchison, "A Low Third Order Intermodulation Amplifier with Harmonic Feedback Circuitry," *1996 IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 827-830.